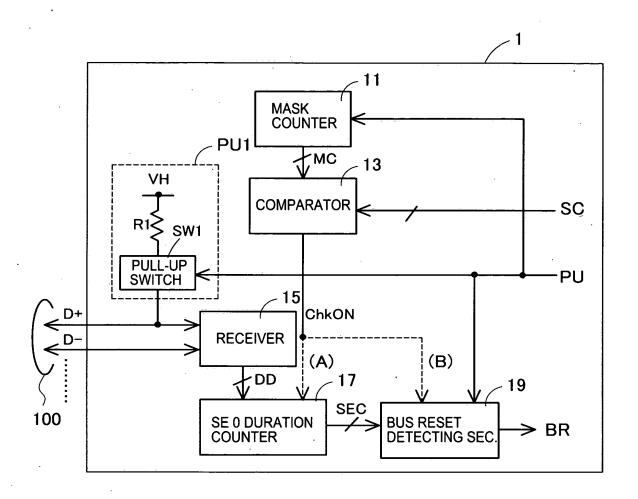
TITLE: TERMINATION CONTROL DEVICE,
AND UNIVERSAL SERIAL BUS
SYSTEM
INVENTORS: Takahiro NIWA
SERIAL NO.:
DOCKET NO.: 1566.1008

FIG.1

## CIRCUIT BLOCK DIAGRAM OF FIRST EMBODIMENT



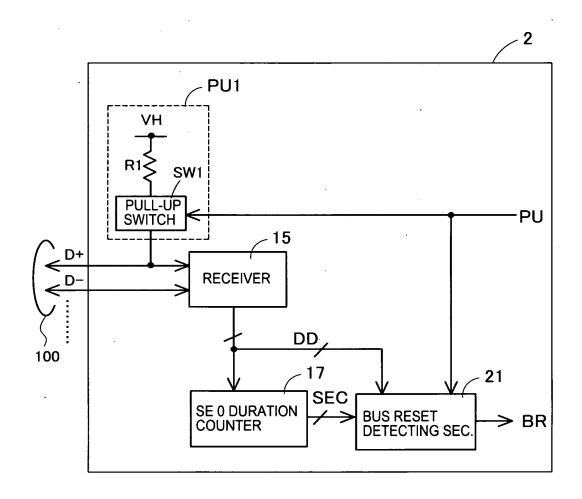
TITLE: TERMINATION CONTROL DEVICE, AND UNIVERSAL SERIAL BUS SYSTEM INVENTORS: Takahiro NIWA SERIAL NO.: DOCKET NO.: 1566.1008 2/5  $2.5\,\mu\,{\rm sec}$  OR LONGER JST SEC SEC BR BR Σ Ğ **∑** ₽ \_  $\mathbb{S}$ 

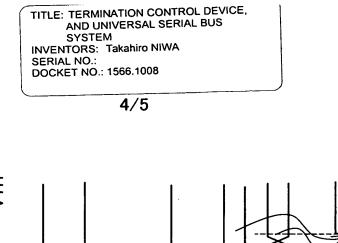
OPERATIONAL WAVEFORM OF FIRST EMBODIMENT

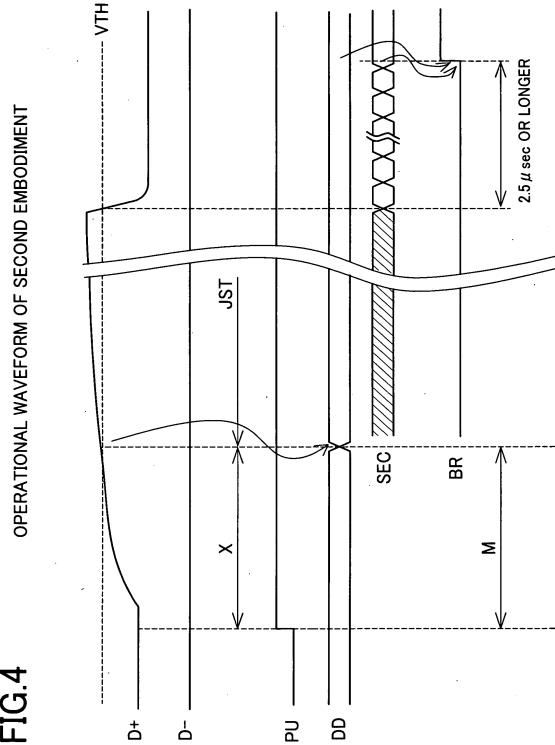
TITLE: TERMINATION CONTROL DEVICE,
AND UNIVERSAL SERIAL BUS
SYSTEM
INVENTORS: Takahiro NIWA
SERIAL NO.:
DOCKET NO.: 1566.1008

FIG.3

## CIRCUIT BLOCK DIAGRAM OF SECOND EMBODIMENT







TITLE: TERMINATION CONTROL DEVICE,
AND UNIVERSAL SERIAL BUS
SYSTEM
INVENTORS: Takahiro NIWA
SERIAL NO.:
DOCKET NO.: 1566.1008

FIG.5

## TERMINATION CIRCUIT OF UNIVERSAL SERIAL BUS

